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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/944,085	09/04/2001	Kazutaka Inukai	12732-073001	3800

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EXAMINER	
SHAPIRO, LEONID	
ART UNIT	PAPER NUMBER
2673	6

DATE MAILED: 06/25/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/944,085	KAZUTAKA ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 September 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3,5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Drawings

1. The drawings are objected to because in Fig. 10B gate signal line driver circuit should be connected to gate signal line instead of source signal line. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: On page 14, Line 15 should have n-1 instead of n+1, the same as on Line 11.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3, 5-7,9-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Someya (US Patent No. 6,040,819) in view of Kane (US Patent No. 6,229,508 B1).

As to claim 1, Someya teaches a method of driving an EL display device including a plurality of pixels, the method comprising: dividing a frame period into n + m display periods (where n and m are both natural numbers), wherein the n + m display periods each correspond to one bit of a digital video signal among n bits of the digital video signal, a plurality of display

periods, among the n + m display periods correspond to the same bit of the digital video signal, and other display periods corresponding to other bits of the digital video signal, among the n + m display periods, appear between the plurality of display periods (See Fig. 6, items SF9-1, SF8-SF1 and SF9-2, in description See Col. 34, Lines 47-57).

Someya does not show first, second and third TFT and an organic EL element, for each of the n+ m display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT and beginning the respective display period by turning off the third TFT; and after each of the n + m display periods begins, completing the respective display period by beginning another display period or by turning on the third TFT; wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off.

Kane teaches first (N1), second (N3) and third (N2) TFT and an organic EL element (See Fig. 5, items N1-N3, 550, in description See Col. 5, Lines 56-59), inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT and beginning the respective display period by turning off the third TFT (See Figs 5-6, items N1-N3, 550, in description See from Col. 5, Line 56 to Col. 6, Line 49); and after each of the n + m display periods begins, completing the respective display period by beginning another display period or by turning on the third TFT (See Figs 5-6, items N1-N3, 550, in description See from Col. 5, Line 56 to Col. 6, Line 49); wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off (See Figs 5-6, items N1-N3, 550, in description See from Col. 5, Line 56 to Col. 6, Line 49). It would have been obvious to one of ordinary skill in the art at the time of the invention to

implement the three TFTs driving method as shown by Kane in the Someya apparatus and method in order to reduce the occurrence of a false profile in a moving image (See Col. 3, Lines 66-67 in the Someya reference) and implement inexpensive pixel structure having three transistors (See Col. 2, Line 14 in the Kane reference).

As to claim 5, Someya teaches a method of driving an EL display device including a plurality of pixels, the method comprising: dividing a frame period into n + m display periods (where n and m are both natural numbers), wherein the n + m display periods each correspond to one bit of a digital video signal among n bits of the digital video signal, a plurality of display periods, among the n + m display periods correspond to the most significant bit of the digital video signal, and other display periods corresponding to other bits of the digital video signal, among the n + m display periods, appear between the plurality of display periods (See Fig. 6, items SF9-1, SF8-SF1 and SF9-2, in description See Col. 34, Lines 47-57).

Someya does not show first, second and third TFT and an organic EL element, for each of the n+ m display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT and beginning the respective display period by turning off the third TFT; and after each of the n + m display periods begins, completing the respective display period by beginning another display period or by turning on the third TFT; wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off.

Kane teaches first (N1), second (N3) and third (N2) TFT and an organic EL element (See Fig. 5, items N1-N3,550, in description See Col. 5, Lines 56-59), inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on

the first TFT and beginning the respective display period by turning off the third TFT (See Figs 5-6, items N1-N3, 550, in description See from Col. 5, Line 56 to Col. 6, Line 49); and after each of the n + m display periods begins, completing the respective display period by beginning another display period or by turning on the third TFT (See Figs 5-6, items N1-N3, 550, in description See from Col. 5, Line 56 to Col. 6, Line 49); wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off (See Figs 5-6, items N1-N3, 550, in description See from Col. 5, Line 56 to Col. 6, Line 49). It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the three TFTs driving method as shown by Kane in the Someya apparatus and method in order to reduce the occurrence of a false profile in a moving image (See Col. 3, Lines 66-67 in the Someya reference) and implement inexpensive pixel structure having three transistors (See Col. 2, Line 14 in the Kane reference).

As to claim 9, Someya teaches a method of driving an EL display device including a plurality of pixels, the method comprising: dividing a frame period into n + m display periods (where n and m are both natural numbers), wherein the n + m display periods each correspond to one bit of a digital video signal among n bits of the digital video signal, upper bits of the digital video signal correspond to a plurality of display periods among the n + m display periods, and other display periods corresponding to other bits of the digital video signal, among the n + m display periods, appear between the plurality of display periods (See Fig. 6, items SF9-1, SF8-SF1 and SF9-2, in description See Col. 34, Lines 47-57).

Someya does not show first, second and third TFT and an organic EL element, for each of the n+ m display periods, inputting the corresponding bit of the digital video signal to a gate

electrode of the second TFT by turning on the first TFT and beginning the respective display period by turning off the third TFT; and after each of the n + m display periods begins, completing the respective display period by beginning another display period or by turning on the third TFT; wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off.

Kane teaches first (N1), second (N3) and third (N2) TFT and an organic EL element (See Fig. 5, items N1-N3,550, in description See Col. 5, Lines 56-59), inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT and beginning the respective display period by turning off the third TFT (See Figs 5-6, items N1-N3, 550, in description See from Col. 5, Line 56 to Col. 6, Line 49); and after each of the n + m display periods begins, completing the respective display period by beginning another display period or by turning on the third TFT (See Figs 5-6, items N1-N3, 550, in description See from Col. 5, Line 56 to Col. 6, Line 49); wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off (See Figs 5-6, items N1-N3, 550, in description See from Col. 5, Line 56 to Col. 6, Line 49). It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the three TFTs driving method as shown by Kane in the Someya apparatus and method in order to reduce the occurrence of a false profile in a moving image (See Col. 3, Lines 66-67 in the Someya reference) and implement inexpensive pixel structure having three transistors (See Col. 2, Line 14 in the Kane reference).

As to claim 13, Someya teaches a method of driving an EL display device including a plurality of pixels, the method comprising: dividing a frame period into n + m display periods

(where n and m are both natural numbers), wherein the n + m display periods each correspond to one bit of a digital video signal among n bits of the digital video signal, a plurality of display periods, among the n + m display periods correspond to the same bit of the digital video signal, and other display periods corresponding to other bits of the digital video signal, among the n + m display periods, appear between the plurality of display periods (See Fig. 6, items SF9-1, SF8-SF1 and SF9-2, in description See Col. 34, Lines 47-57).

Someya does not show first, second TFT and an organic EL element, for each of the n+ m display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT; and after each of the n + m display periods begins, completing the respective display period by beginning another display period; wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off.

Kane teaches first (N1), second (N2) and an organic EL element (See Fig. 2, items N1-N2, LED, in description See Col. 1, Lines 46-53), for each of the n+ m display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT; and after each of the n + m display periods begins, completing the respective display period by beginning another display period; wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off (See Fig. 2, items N1-N2, LED, in description See Col. 1, Lines 46-53). It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the two TFTs driving method as shown by Kane in the Someya apparatus and method in order to reduce the occurrence of a false profile in a moving image (See Col. 3, Lines 66-67 in the Someya reference) and

implement inexpensive pixel structure having three transistors (See Col. 2, Line 14 in the Kane reference).

As to claim 17, Someya teaches a method of driving an EL display device including a plurality of pixels, the method comprising: dividing a frame period into n + m display periods (where n and m are both natural numbers), wherein the n + m display periods each correspond to one bit of a digital video signal among n bits of the digital video signal, a plurality of display periods, among the n + m display periods correspond to the most significant bit of the digital video signal, and other display periods corresponding to other bits of the digital video signal, among the n + m display periods, appear between the plurality of display periods (See Fig. 6, items SF9-1, SF8-SF1 and SF9-2, in description See Col. 34, Lines 47-57).

Someya does not show first, second TFT and an organic EL element, for each of the n+ m display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT; and after each of the n + m display periods begins, completing the respective display period by beginning another display period; wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off.

Kane teaches first (N1), second (N2) and an organic EL element (See Fig. 2, items N1-N2, LED, in description See Col. 1, Lines 46-53), for each of the n+ m display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT; and after each of the n + m display periods begins, completing the respective display period by beginning another display period; wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off (See

Fig. 2, items N1-N2, LED, in description See Col. 1, Lines 46-53). It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the two TFTs driving method as shown by Kane in the Someya apparatus and method in order to reduce the occurrence of a false profile in a moving image (See Col. 3, Lines 66-67 in the Someya reference) and implement inexpensive pixel structure having three transistors (See Col. 2, Line 14 in the Kane reference).

As to claim 21, Someya teaches a method of driving an EL display device including a plurality of pixels, the method comprising: dividing a frame period into n + m display periods (where n and m are both natural numbers), wherein the n + m display periods each correspond to one bit of a digital video signal among n bits of the digital video signal, upper bits of the digital video signal correspond to a plurality of display periods among the n + m display periods, and other display periods corresponding to other bits of the digital video signal, among the n + m display periods, appear between the plurality of display periods (See Fig. 6, items SF9-1, SF8-SF1 and SF9-2, in description See Col. 34, Lines 47-57).

Someya does not show first, second TFT and an organic EL element, for each of the n+ m display periods, inputting the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT; and after each of the n + m display periods begins, completing the respective display period by beginning another display period; wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off.

Kane teaches first (N1), second (N2) and an organic EL element (See Fig. 2, items N1-N2, LED, in description See Col. 1, Lines 46-53), for each of the n+ m display periods, inputting

the corresponding bit of the digital video signal to a gate electrode of the second TFT by turning on the first TFT; and after each of the n + m display periods begins, completing the respective display period by beginning another display period; wherein the organic EL element emits light when the second TFT is turned on, and does not emit light when the second TFT turned off (See Fig. 2, items N1-N2, LED, in description See Col. 1, Lines 46-53). It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the two TFTs driving method as shown by Kane in the Someya apparatus and method in order to reduce the occurrence of a false profile in a moving image (See Col. 3, Lines 66-67 in the Someya reference) and implement inexpensive pixel structure having three transistors (See Col. 2, Line 14 in the Kane reference).

As to claims 2,6,10,14,18 and 22, Kane teaches the first and second TFT have the same polarity (See Fig. 2, items N1-N2 and Fig. 5, items N1, N3).

As to claims 3,7,11,15,19 and 23, Someya teaches Tr1, Tr2, Tr3, ... Trn-1 = 2^0,2^1,2^2, ... ,2^{n-2},2^n , where the lengths of the display periods, among the n-m display periods, corresponding to respective bits of the digital video signal are taken as Tr1, Tr2, Tr3, ... Trn-1,Trn (Fig.9, items SF1-SF8, in description See Col. 1, Lines 10-35).

As to claims 12,16 and 20, Kane teaches the first TFT function as a switching TFT and the second TFT function as an EL driver TFT (See Fig. 2, items N1-N2, LED, in description See Col. 1, Lines 46-53).

4. Claims 4, 8 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Someya and Kane as aforementioned in claims 1, 5 and 9 in view of Kanatani et al. (US Patent No. 4,070,663).

Kane teaches the first TFT function as a switching TFT (See Fig. 5, item 530, in description See Col. 5, Line 59-60), the second TFT function as an EL driver TFT (See Fig. 5, item 510, in description See Col. 5, Line 59-60), and third TFT function as a TFT, connected to Autozero line (See Fig. 5, item 520, in description See Col. 5, Line 61-62).

Someya and Kane do not show third TFT connected to the erase line.

Kanatani et al. teaches erasing data line (See Fig. 25, item j, in description See Col. 19, Lines 37-54). It would have been obvious to one of ordinary skill in the art at the time of the invention to replace Autozero line with erase line as shown by Kanatani et al. in the Someya and Kane apparatus and method in to implement inexpensive pixel structure having three transistors (See Col. 2, Line 14 in the Kane reference).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

The Stewart (US Patent No. 5,302,966) reference discloses active matrix EL display and method of operation.

The Dawson et al. (US Patent No. 6229,506 B1) reference discloses active light emitting diode pixel structure and concomitant method.

The Knapp et al. (US Patent No. 6,373,454 B1) reference discloses active matrix EL display devices.

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4750.

ls
June 7, 2003

VIJAY SHANKAR
PRIMARY EXAMINER